AMENDMENTS TO THE DRAWINGS:

The attached sheets of drawings include changes to Figs. 1(a)-1(c), 2(d)-2(f), 3, 4 5(a), 6.

The sheet which includes Figs. 1(a)-1(c) replaces the original sheet including Figs. 1(a)-1(c). The lead lines requested by the Examiner have been added.

The sheet which includes Figs. 2(d)-2(f) replaces the original sheet including Figs. 2(d)-2(f). The brackets have been removed from the figures as requested by the Examiner.

The sheet which includes Figs. 3 and 4 replaces the original sheet including Figs. 3 and 4. The bracket has been removed from Figure 3 and a lead line from reference designation 3 has been added as requested by the Examiner. In Figure 4 the bracket has been removed.

The sheet which includes Figs. 5(a) and 6 replaces the original sheet including Figs. 5(a) and 6. The height reference designation "h" has been added and a lead line from reference number 30 has also been added. In Figure 6 the bracket has been removed.

Attachment: Replacement Sheets

Annotated Sheets Showing Changes

REMARKS

In regard to the Examiners objections to the drawings, Applicants have modified Figure 5(a) to include the height designation "h" and additionally applicants have modified the specification on page 20 in the second full paragraph to reflect the fact the height "h" reference is in Figure 5(a) and not Figure 5(b). Applicants have also eliminated the use of brackets as required by the Examiner. Additionally, Applicants have modified the drawings to include the requisite lead lines for Figure 3 as identified by the Examiner.

In regard to the objections to Figures 1(b) and (c) Applicants note that because the structure is flipped as described in the specification in the final paragraph on page three which states that the semiconductor module unit is reversed by the mounter. Accordingly, the Applicants submit that the illustrations of Figures 1(b) and 1(c) need not be changed and indeed accurately reflect the different board structures.

In regard to Figure 4, Applicants note that reference characters 3 and 19 are actually distinct elements. Reference 3 is directed to overall assembly jig and 19 is the layering space as noted in the specification. The reversing or flipping of the structure described above also obviates the Examiners issues raised on page 3 of the action with reference to the objections under 37 CFR section 1.84(p)(4). Accordingly these objections should be withdrawn as well. If the Examiner still believes that there is an outstanding unresolved issue then the undersigned requests that the Examiner conduct a telephone interview.

Applicants submit that these changes and remarks overcome all of the drawing objections. In regard to the assertion that there is no box-shaped member positioned on a base, Applicants submit that Figure 2(e) as well as Figure 4 each clearly illustrate such a structure. The same is also true for the subject matter of claim 3, and that these elements are adequate described in the specification. Similarly, with regard to the Examiner's objections under 37 CFR section 1.83(a) of claims 6, 7, 12, and 13 as well as the rejections under section

112, first paragraph as to all claims Applicants submit that each of the referenced elements are clearly present in the specification. For example, the box-shaped element is reference 14 that is located on the base member 5. The height restriction mechanism is clearly illustrated in Figure 2(d) as element 17 which is also described in detail in the specification. All that the Examiner has done is make the bald unsupported allegation that all of the elements of the claims are not described in the specification and there is simply no foundation for these assertions and the rejections under section 112 should be withdrawn. Indeed, the specification actually uses the term "box-shaped" see page 15 in the second full paragraph. There is simply no foundation whatsoever for these rejections and objections and they should be withdrawn.

In regard to the remaining elements asserted to be lacking in description, Applicants note that the specification describes a number of embodiments and the limitations referenced in the claims may actually relate to different structures in the various embodiments. By way of example, Applicants note that the lateral position restriction mechanism in one embodiment is found in the side walls of the "box- shaped" member 16. This is described on pages 15-16 wherein "an inner surface" of the box-shaped member "restricts an outer periphery of the semiconductor modules 2 . . . See specifically the second full paragraph on page 15 through the top line of page 16. Alignment is performed by the pin members described in the specification such as the pin 22.

Applicants also request reconsideration of the Examiner's rejections under section 112 second paragraph for allegedly omitting essential structural elements. Applicants submit that no elements are missing and the specification clearly describes the subject matter so that a person of ordinary skill in the art will readily understand the subject matter of the invention.

Applicants respectfully request reconsideration of Examiner's rejection of Claims 1 – 7 and 11-13 under 35 U.S.C. §102 as being unpatentable over Levy (U.S. Patent No. 5,869,353). Levy is directed to the apparatus of a multi-chip module such that Integrated Circuits (ICs) that fit within a pre-defined aperture of a panel can be bonded together at edges directly to an IC above or below it. Applicants assert this method and device to be entirely distinct from Applicant's currently claimed invention.

For example, Levy discloses a collection 12 of frames 22 to be used in the positioning of semiconductor IC's into pre-defined panel apertures to create a vertically aligned chip package stack. Applicant's invention, however, discloses the use of an assembly jig 3 in the creation of a multi-layered semiconductor device including multiple layers of printed wiring boards and semiconductor ICs. Further, Levy discloses that connections between IC layers be done solely via soldering of the pads 26 and leads 16 on the outside perimeter of the ICs (See Figures 5 and 6). Applicant's invention, however, discloses connections between layers be done via solder bumps 13, and lands 8,9 positioned below or above the printed wiring board or IC (See Figures 2 – 6).

To state it another way, Applicant's current invention would not be in any way applicable to Levy because 1) Levy does not use printed circuit boards between layers that are subject to warping during the reflow step, and 2) Levy requires the dimensions of the semiconductor chips to be within the dimensions of the aperture opening, and therefore does not need to control the height of the device as one does with Applicant's multilayer semiconductor package.

Therefore, Levy provides no teaching or suggestion towards Applicant's currently claimed invention, which provides for an assembly jig to restrict the height of the resulting multi-layered semiconductor module to a consistent and repeatable value, and to suppress deformation due to warp of the layered printed circuit boards. As a result, Applicant's invention improves the yield and productivity in the creation of these multilayer semiconductor devices while incurring minimum additional costs.

Applicants have added new claims that alternately define the invention solely for the purpose of advancing prosecution.

In conclusion, and based upon the above amendments and remarks, Applicants respectfully submit that all claims now stand in condition for allowance.

Respectfully submitted,

Date: 12/7/04

(Reg. #37,607)

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Attorney for Applicant

ANNOTATED DRAWINGS

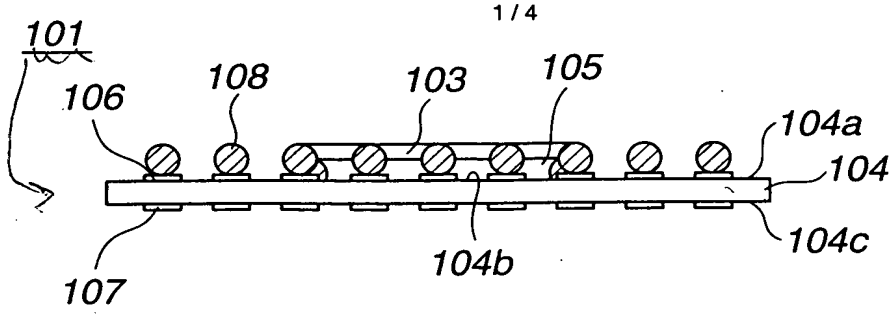

FIG.1(a)

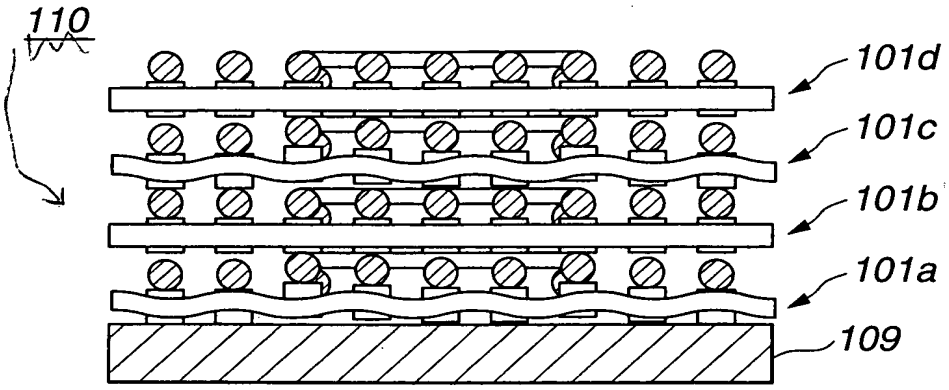

FIG.1(b)

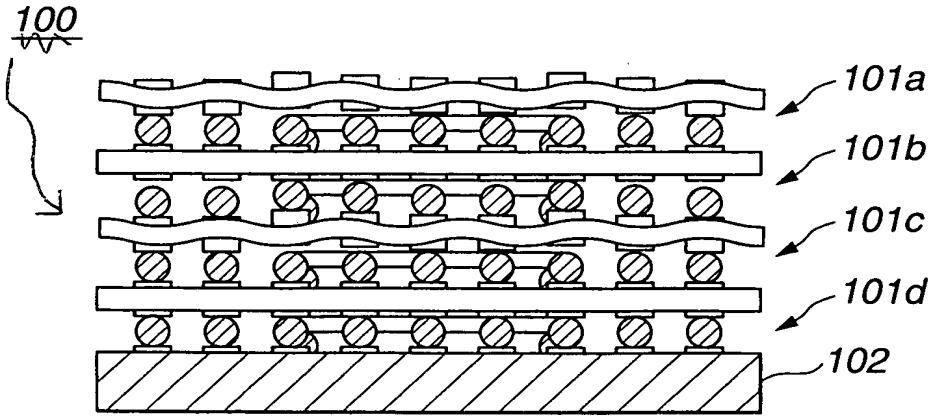

FIG.1(c)

FIG.2(a)

FIG.2(b)

FIG.2(c)

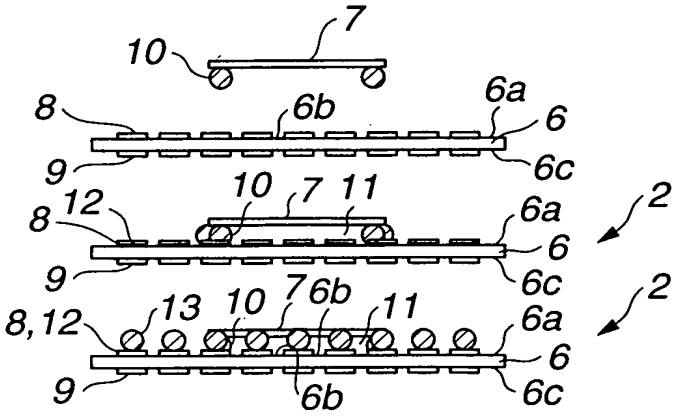

FIG.2(d)

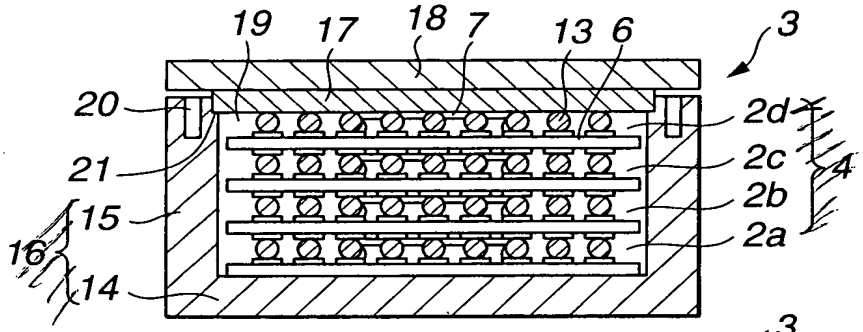

FIG.2(e)

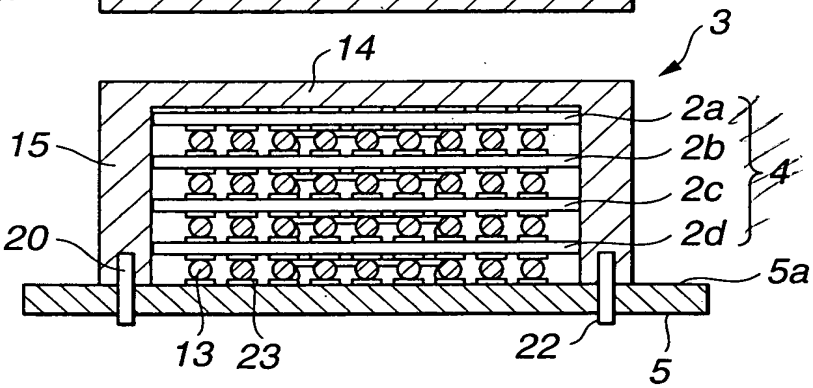

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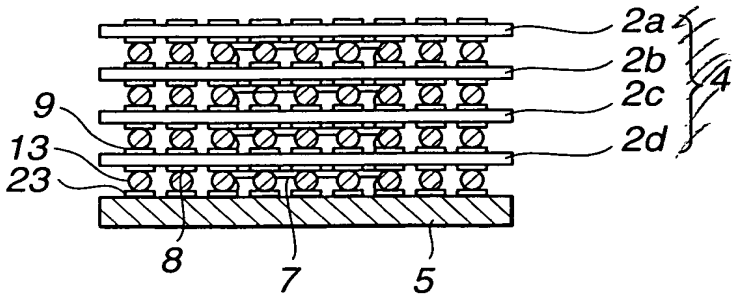
FIG.2 (f)



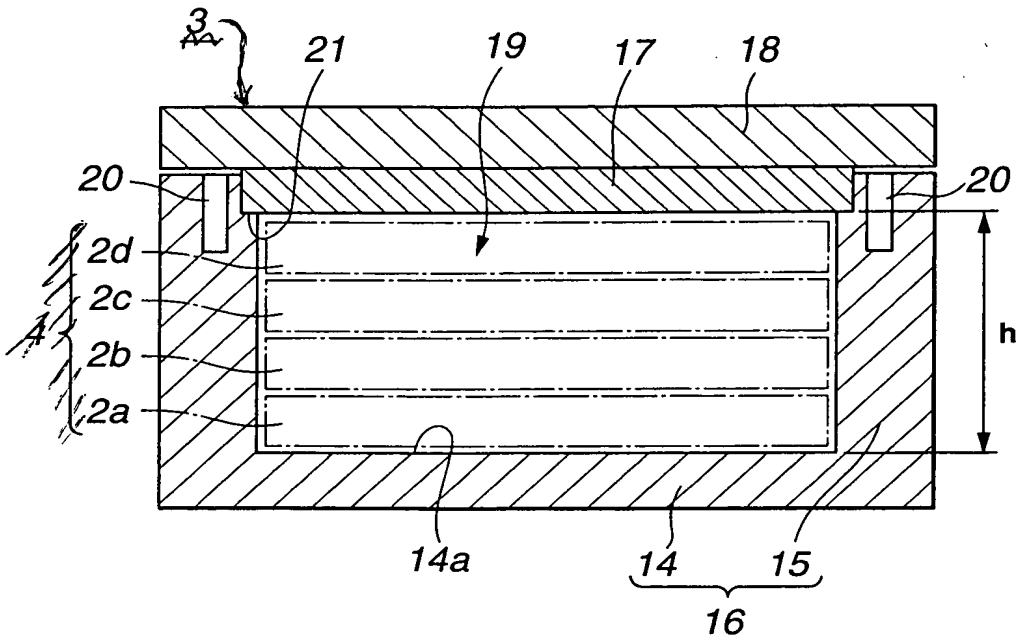

3
21
19
17
18
20
20
2d
2c
2b
2a
4
h
14a
14
15
16

FIG.3

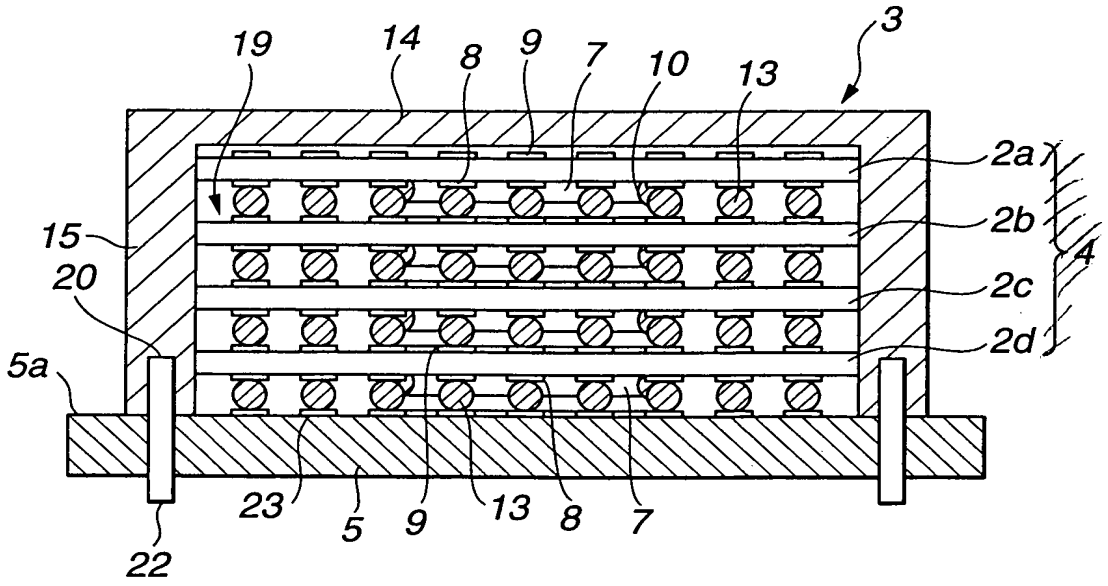

19
14
8
9
7
10
13
3
2a
2b
2c
2d
4
15
20
5a
23
5
9
13
8
7
22

FIG.4

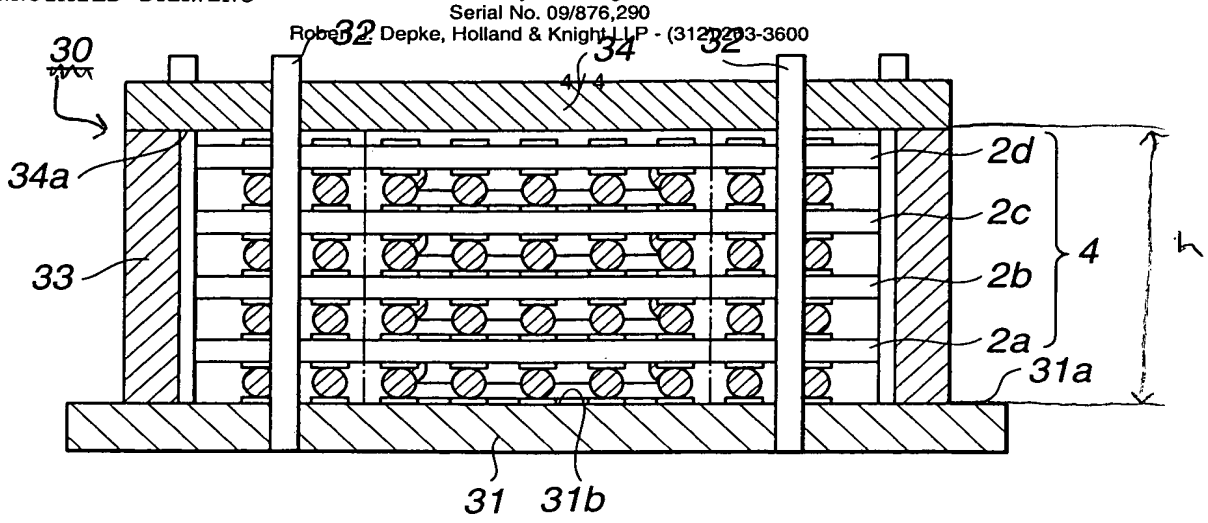


FIG.5(a)

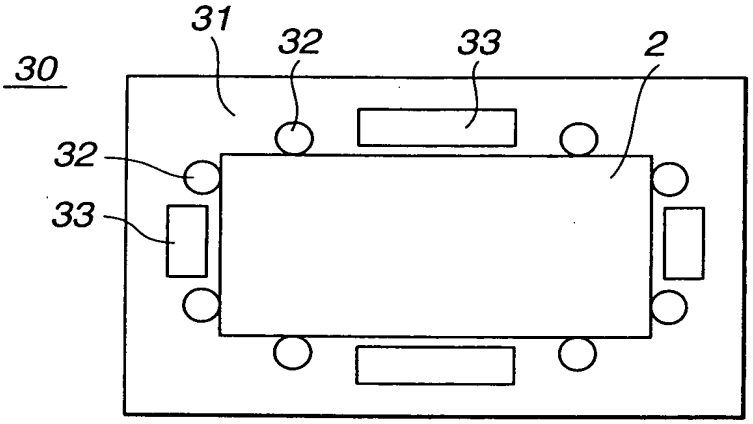


FIG.5(b)

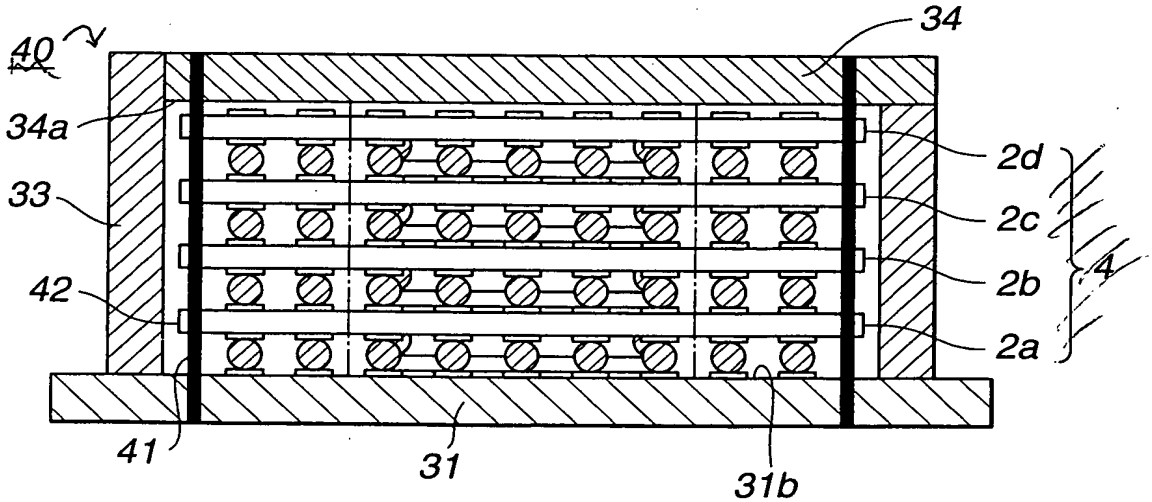


FIG.6